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Question Paper Code : 80531

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2024.

Fifth Semester

Electronics and Communication Engineering

EC 8552 — COMPUTER ARCHITECTURE AND ORGANIZATION

(Common to : Electronics and Telecommunication Engineering)

(Regulations 2017)

Time : Three hours   Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is the basic principle behind to move from uniprocessor to multi-processor?

2. What is the difference between operation and operands?

3. How to create n bit ripple carry adder using normal full adder and half adders?

4. For floating point division, what are the algorithms used?

5. What do you mean by structural hazard?

6. What do you mean by exception?

7. Neatly draw and show the memory hierarchy between main memory and cache memory.

8. In a 32 bit system, what will be the size of virtual memory?

9. Define multithreading. What is multithreaded processor?

10. Show different stages of graphics pipeline in a modern CPU.

PART B — (5 × 13 = 65 marks)

11. (a) Briefly describe about various shift operations available in simple computer Risc category processors.

Or

(b) Discuss about various load and store instructions available in MIPS programming.

12. (a) Explain about Booth's multiplier algorithm and multiply 2 × 3 using Booth's algorithm.

Or

(b) Briefly depict the non-restoring division process and divide two 4-bit numbers: 7(0111)/3 (0011) using non-restoring division processes.

13. (a) How many types of hazards occur in a system? Describe all with suitable examples.

Or

(b) Briefly describe pipelined datapath and its important components.

14. (a) Describe the basic cache operations. Briefly describe fully associative cache with neat diagram.

Or

(b) Describe in detail, how to implement virtual memory with paging with neat block diagram.

15. (a) Describe in detail regarding different types of multithreading with neat diagrams.

Or

(b) Briefly describe about Flynn's proposed various multiprocessor techniques.

PART C — (1 × 15 = 15 marks)

16. (a) Assume that you are given a machine with an unknown configuration. You need to find out a host of cache parameters by measuring the time it takes to execute different programs. These programs will be tailor made in such a way that they will reveal something about the underlying system. Describe the approach by assuming that the caches follow the LRU scheme for replacement.

  (i) How will you estimate the size of the L1 cache? (5)

  (ii) How will you estimate the L1 block size? (5)

  (iii) How will you estimate the L1 cache associativity? (5)

Or

  (b) Write a MIPS assembly program to find the greatest common divisor of two binary numbers u and v. Assume the two inputs (positive integers) to be available in $r3$ and $r4$. Store the result in $r5$.

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