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Question Paper Code : 50575

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2024.

Fifth/Sixth Semester

Electronics and Communication Engineering

CEC 361 – VALIDATION AND TESTING TECHNOLOGY

(Common to : Electronics and Telecommunication Engineering)

(Regulations 2021)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Name two processes involved in VLSI fabrication, and explain their significance in the manufacturing of integrated circuits.

2. What are the key technologies discussed related to IC technology, and can you briefly define each of them?

3. What is the I_{DS}-V_{DS} relationship in a MOS transistor?

4. Mention the significance of "G_{DS}" in MOS circuits.

5. What is a pass transistor, and how is it different from a regular CMOS switch?

6. Write about the basic operation of an NMOS inverter.

7. How do you calculate delays in CMOS circuits?

8. What is sheet resistance (Rs), and how is it relevant to MOS devices?

9. What are the objectives of testing in VLSI design?

10. Define "fault coverage" and explain its importance in silicon validation.

PART B — (5 × 13 = 65 marks)

11. (a) Discuss the significance of oxidation in VLSI fabrication and how it contributes to the overall performance of integrated circuits.

Or

(b) Examine the role of integrated resistors and capacitors in modern IC technology, considering their impact on circuit design and functionality.

12. (a) Explain the $I_{DS} - V_{DS}$ relationship in MOS transistors in detail.

Or

(b) Discuss the effects of short-channel and narrow-channel width on MOS transistors.

13. (a) Explain the working principles and applications of pass transistors and transmission gates in digital circuits.

Or

(b) Compare and contrast different pull-up structures commonly used in CMOS technology. Provide practical examples to illustrate the impact of design choices on power consumption, speed, and noise immunity.

14. (a) Explain the significance of sheet resistance (Rs) and conductivity in MOS devices.

Or

(b) Discuss in detail the concept of logical effort and its importance in CMOS circuit design.

15. (a) Explain the various levels of testing in ensuring the reliability and functionality of VLSI circuits.

Or

(b) Describe the different types of testing in VLSI, such as functionality tests, silicon debug, and manufacturing tests.

PART C — (1 × 15 = 15 marks)

16. (a) You are tasked with designing a high-performance CMOS circuit that needs to operate at a low power consumption while driving a large capacitive load. Describe the design considerations you would take into account.

Or

(b) As a semiconductor manufacturing manager, you've been tasked with improving the efficiency and reliability of the silicon validation and testing process for a cutting-edge VLSI chip. Describe your overall strategy, considering the need for testing, objectives, equipment, and economic factors.