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Question Paper Code : 80512

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2024.

Sixth/Seventh Semester

Electronics and Communication Engineering

EC 8095 – VLSI DESIGN

(Common to: Electrical and Electronics Engineering/Electronics and Instrumentation Engineering/Electronics and Telecommunication Engineering/Instrumentation and Control Engineering/Robotics and Automation)

(Regulations 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Realize the CMOS inverter.

2. Define noise margin.

3. Write any four circuit pitfalls that can cause chips to fail.

4. How bubble pushing with DeMorgan's law for two input NAND and NOR is performed?

5. Differentiate positive latch and negative latch.

6. What is clock jitter and clock skew?

7. Mention few features of carry-lookahead adder.

8. Give the three common types of variable shifts with an example.

9. Mention the integrated circuits design style classification.

10. State the need for testing in VLSI?

PART B — (5 × 13 = 65 marks)

11. (a) (i) Implement the two input AND gate using transmission gates and explain the operation. (6)

(ii) What are the three regions of operation of MOS transistor? Obtain the drain current in three regions of operation. (7)

Or

(b) (i) Explain the DC characteristics for the static CMOS inverter. (7)

(ii) Realize the n-input NAND gate with parasitic delay and find the Elmore delay. (6)

12. (a) (i) Draw and explain the generalized structure of the Cascade Voltage Switch Logic (CVSL). Show how AND and NAND gates are realized using CVSL. (7)

(ii) What are transmission gates? Draw the effective resistance of a unit transmission gate. Realize the 2:1 multiplexer using transmission gates and explain the operation. (6)

Or

(b) Obtain the expression for total power of the CMOS circuit based on static and dynamic power operations. (13)

13. (a) (i) Design a multiplexer based latch using transmission gates and master slave edge triggered register using positive and negative latch. (7)

(ii) What is true single phase clocked circuits (TSPC) for positive and negative latch? Design the AND latch using TSPC. (6)

Or

(b) (i) Describe the operation CMOS Schmitt trigger with illustrations. (7)

(ii) Design the CMOS pulsed latches and explain the operation. (6)

14. (a) (i) Design a 4-bit carry generation and propagation adder. (7)

(ii) Illustrate the generation, shifting and summing of partial products in a 6 × 6 bit Multiplier. (6)

Or

(b) (i) Describe the 6T SRAM cell for read and write operation. (6)

(ii) Elucidate the simplest design with one row per word and one column per bit and two-way fold with eight rows and eight columns. (7)

15. (a) (i) Illustrate the overview of FPGA architecture. (7)

(ii) In design for manufacturability, discuss the ways to optimize circuits to increase their yield. (6)

Or

(b) Discuss in detail the scan design strategy for testing to provide observability and controllability at each register. (13)

PART C — (1 × 15 = 15 marks)

16. (a) (i) Realize the complex and-or-invert structure Y=(A.(B+C) + D.E)' using CMOS logic and pseudo nMOS logic. (8)

(ii) What is the monotonicity in dynamic gates? Provide the solution to overcome the monotonicity. (7)

Or

(b) (i) Apply the 3-stage pipelining for log(|an+bn|), where n=1,2,3,4,5. Find the total clock period required to get all the outputs for n=1,2,3,4,5. (8)

(ii) Estimate the delays of 8:256 decoders using static CMOS and footed domino gates. Assume the decoder has an electrical effort of H=10 and that both true and complementary inputs are available. (7)