Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 51008

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2024.

Third Semester

Electrical and Electronics Engineering

EE 3302 — DIGITAL LOGIC CIRCUITS

(Common to PTEE 3302 – Digital Logic Circuits for B.E. (Part-Time) First Semester – Electrical and Electronics Engineering – Regulations 2023)

(Regulations 2021)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert the number $(255)_{10}$ in to binary format.
2. What is the largest binary number that can be expressed with 7 bits? What is its equivalent decimal value?
3. Draw 8 × 1 multiplexer using only 4 × 1 multiplexers.
4. State any two differences between Multiplexer and Demultiplexer.
5. The output Qn of a JK flip-flop is zero. It changes to 1 when a clock pulse is applied. What are the inputs at J and K?
6. List down the terminal count of a 8 bit binary counter in up-mode and down-mode.
7. Sketch the generic architecture of CPLD.
8. Justify the statement, "Race around condition that exist in flip flops can be eliminated".
9. When can RTL be used to represent digital systems?
10. Write VHDL code for half adder in data flow model.

PART B — (5 × 13 = 65 marks)

11. (a) (i) What are the applications of Gray code? (4)

(ii) Convert the following numbers into Gray code numbers.

$(89)_{10}$

$(54)_{16}$

$(145)_8$ (9)

Or

(b) Given the 8-bit data word 11000100, generate the 13-bit composite word for the Hamming code that corrects single errors and detects double errors.

12. (a) Use Quine-McCluskey principle to simply the following expression $f = \sum m(1, 2, 3, 5, 6, 7, 8, 9, 12, 13, 15)$ and implement using logic Gates.

Or

(b) Design a 4-bit gray to binary code converter using K-map.

13. (a) With a neat diagram explain the working of bidirectional shift register.

Or

(b) Design and draw the logic diagram of Mod-12 synchronous counter using JK flip-flops.

14. (a) Design a circuit with optimum utilization of PLA to implement the following functions $F1 = \sum m(0, 2, 5, 8, 9, 11)$, $F2 = \sum m(1, 3, 8, 10, 13, 15)$, $F3 = \sum m(0, 1, 5, 7, 9, 12, 14)$.

Or

(b) Implement a full adder using PAL and ROM.

15. (a) Write an HDL dataflow description of a 4-bit adder, subtractor of unsigned numbers. Use the conditional operator.

Or

(b) Develop a VHDL code for Binary UP/ DOWN counter using JK flip flops.

PART C — ($1 \times 15 = 15$ marks)

16. (a) Derive the PLA programming table for a combinational circuit that squares a 4-bit number and minimize the number of product terms. What is the width of the output?

Or

(b) A synchronous sequential machine has a single control input x, the clock and two Outputs A and B. On consecutive rising edges of the clock, the code on A and B changes from 00 to 01 to 10 to 11 and repeats itself if $x = 1$; if at any time $x = 0$, it holds to the present state. Draw the state diagram, design and implement the circuit using T flip flop.