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Question Paper Code : 20522

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2023.

Fifth Semester

Electronics and Communication Engineering

CEC 334 — ANALOG IC DESIGN

(Common to Electronics and Telecommunication Engineering)

(Regulations 2021)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. For the circuit in Fig.1, Show the on-resistance of M1 as a function of V_G. Assume $\mu_n C_{ox} = 50\mu A / v^2 . W / L = 10$ and $V_{th} = 0.7$. Note that the drain terminal is open.

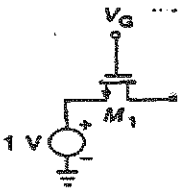


Fig.1

2. Find the voltage gain of the circuit shown in Fig.2 Assume I_0 is ideal.

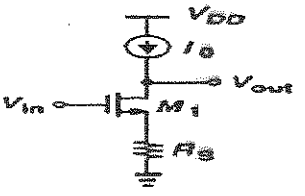


Fig. 2

3. Explain why ringing in step response of a source follower with heavy capacitive load?

4. Find the maximum noise voltage that a single MOSFET can generate.

5. List the benefits and properties of negative feedback circuits.

6. Define slew rate.

7. Define Barkhausen criterian.

8. Show the root locus for a one-pole system.

9. Illustrate on stuck_at_1 and stuck_at_0 faults in two-input AND gate.

10. List the advantage of scan path approach for sequential circuits.

PART B — (5 × 13 = 65 marks)

11. (a) Solve the voltage gain expression for the common source amplifier using

(i) Resistive load

(ii) Diode-connected load

(iii) Current-source load.

Or

(b) (i) Solve the exact voltage gain of the circuit shown in Figure. 2. (7)

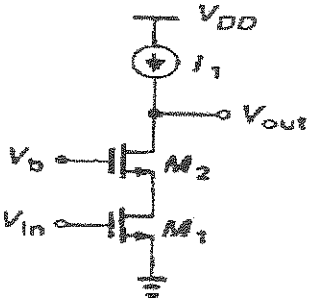
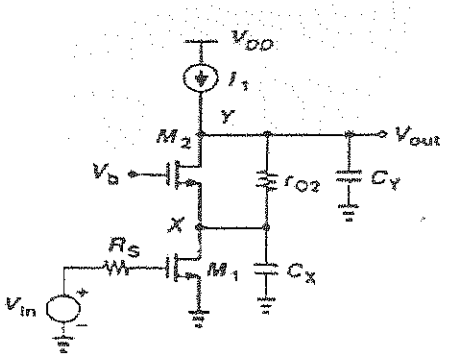


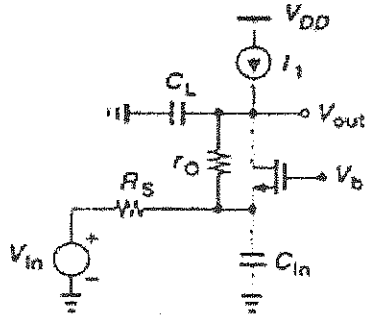
Figure. 2

(ii) Show that the output impedance of the folded cascade amplifier is lower than that of non-folded circuit. (6)

12. (a) (i) Consider the cascade stages shown in Figure., where the load resistance is current source. Neglecting the capacitances associated with M1 representing Vin and M1 by a Norton equivalent. Assume $\gamma = 0$. Compute the transfer function. (7)



(ii) For the common-gate stage shown in Figure, Find the transfer function and input impedance z_{in}. Explain why Z_{in} becomes independent of C_L as this capacitance increases. (6)



Or

(b) (i) For an NMOS current source, calculate the total thermal and 1/f noise in the drain current for a band from 1kHz to 1 MHz. (7)

(ii) For a 100-μm MOS device with $g_m = 1/(100\,\Omega)$, the 1/f noise corner frequency is measured to be 500kHz. If t_{ox} 90 Å, what is the flicker noise coefficient in this technology? (6)

13. (a) Explain in detail about the effect of loading in all the four feedback networks.

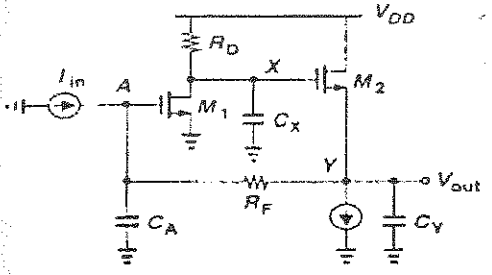
Or

(b) (i) Analyze the effects of various noise that exist in Op-Amp. (7)

(ii) Explain how gain can be boosted in op-amp circuits? (6)

14. (a) (i) An amplifier has a forward gain of A0 = 1000 and two poles at ω_{p1} and ω_{p2}. For $\omega_{p1} = 1$ MHz, find the phase margin of a unity gain feedback loop if (1) $\omega_{p2} = 2\omega_{p1}$ (2) $\omega_{p2} = 2\omega_{p1}$ (2) $\omega_{p2} = 4\omega_{p1}$. (7)

(ii) Consider the transimpedance amplifier shown in Fig. where $Rd = 1k\Omega$, $Rf = 10k\Omega, gm1 = gm2 = (1/100\Omega)$ and $C_A = C_x = C_y = 100fF$. Neglecting all other capacitance and assuming $\lambda = \gamma = 0$ compute the phase margin of the circuit. (6)



Or

(b) Explain in detail about the two-stage op-amps with necessary diagrams.

15. (a) Explain the following (i) undetectable faults (ii) Equivalent faults (iii) Temporary faults with examples.

Or

(b) (i) Explain how multiplexers and tristate drivers are used to enhance testability. (7)

(ii) Discuss on random access scan techniques with neat sketch. (6)

PART C — (1 × 15 = 15 marks)

16. (a) Explain the block diagram of boundary scan architecture and its cell with the help of neat sketch.

Or

(b) Explain in detail for a faulty and fault-free full adder circuit using suitable method.
