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Question Paper Code : 20550

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2023.

Fifth Semester

Electronics and Communication Engineering

CEC 362 — VLSI TESTING AND DESIGN FOR TESTABILITY

(Common to Electronics and Telecommunication Engineering)

(Regulations 2021)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is benefit to cost ratio in a test economics?
2. Neatly draw a typical logic BIST structure.
3. What is scan design in a DFT based approach?
4. What is the basic function of LFSR and MISR?
5. What is concurrent BIST in a memo BIST technique?
6. What is the basic job of Test Control (TC) in a scan design technique?
7. Define hardware partitioning or physical segmentation.
8. What is a combinational ATPG?
9. What is the basic job of BIST controller in a transparent memory BIST test?
10. For testing whom, we need the PLL bypass mechanism.

PART B — (5 × 13 = 65 marks)

11. (a) Neatly show arc describe BIST hierarchy as well as BIST implementation in a random logic test process.

Or

(b) Describe power concern during testing and how power has been managed in this critical situation?

12. (a) Briefly describe the STUMPS architecture for testing with neat diagram.

Or

(b) Describe how LFSR helps to test a functional ROM chip?

13. (a) Neatly draw and describe test architecture for an SoC.

Or

(b) Briefly describe regarding non-invasive and pin-permission modes in a boundary scan.

14. (a) Briefly describe the D-calculus and D-algorithm (Roth) used for ATPG algorithms.

Or

(b) Write some good design practices in an Ad-hoc DFT methods.

15. (a) Distinguish between defect test and performance test in a testing process.

Or

(b) Describe regarding DAC transfer function error and ADC transfer function error.

PART C — (1 × 15 = 15 marks)

16. (a) Multi-tone testing. Figure 16 (a) shows a typical set-up for DSP-based multi-tone testing of a device-under-test (DUT.)

(i) The primitive frequency for testing is $\Delta = 20 H_2$ and the test waveform frequency is F_t = 2020 H_z. What DSP ATE sampling frequency F_s will guarantee 600 unique samples during coherent testing?

(ii) Unfortunately, this sampling frequency leads to a very expensive analog tester. Please explain how to nearly halve the required sampling frequency, while still guaranteeing 600 unique samples, and recompute Δ, M, N, and F_s.

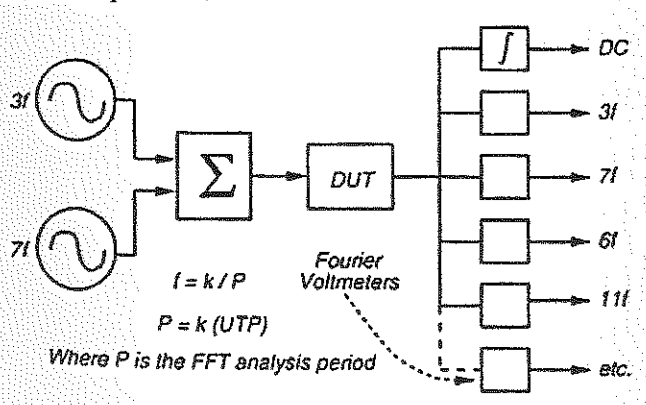

Figure – 16 (a)

Or

(b) Figure 16 (b) shows a 3-bit counter designed using small scale logic Assuming that the only externally available inputs are the clock and reset and the only available outputs are the count bits. Attempt to develop a test for s-s-a faults in the combinational logic that does not cycle the counter through all its states.

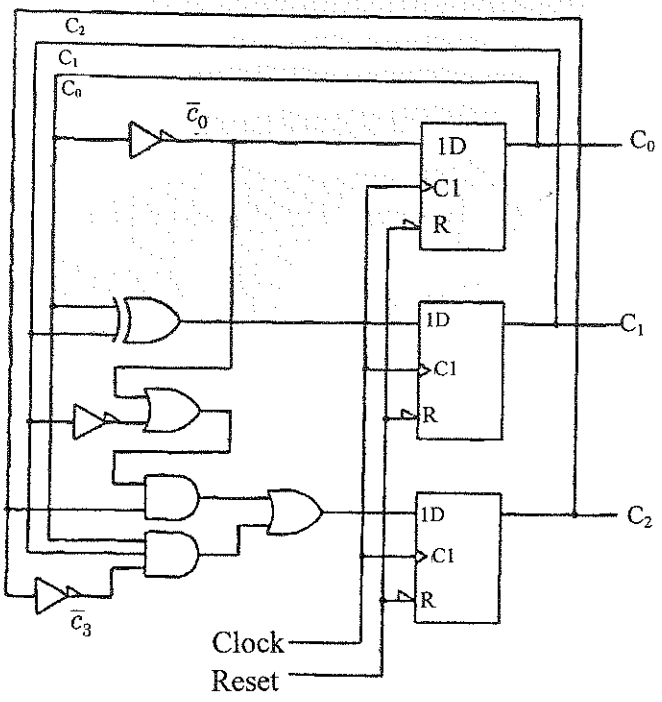

Figure – 16 (b)