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Question Paper Code : F 20558

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2023.

Fifth Semester

Electronics and Communication Engineering

CEC 370 – LOW POWER IC DESIGN

(Common to Electronics and Telecommunication Engineering)

(Regulations 2021)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Describe low-power circuits and explain their significance in electronic design.

2. What are the key advantages of designing low-power circuits in portable electronic devices?

3. Define Dynamic Voltage Scaling (DVS) in the context of low-power design.

4. Briefly explain the significance of Clock Gating as a low-power design technique.

5. State the functions of Low-Voltage Low-Power Adders.

6. State the Significance of Low-Voltage Low-Power Adders in Integrated Circuits.

7. Name two common multiplier architectures used in digital circuit design.

8. Briefly explain the working principle of a Booth multiplier.

9. List two Techniques Used in Low Power SRAM Design.

10. Mention one application where Low-Power ROM Technology is crucial and explain why?

PART B — (5 × 13 = 65 marks)

11. (a) Define leakage power and explain its significance in low-power circuit design.

Or

(b) Describe different techniques for power optimization in CMOS circuits.

12. (a) Explain the role of process technology in low-power design. How do different process technologies affect power consumption.

Or

(b) How can we use power-gating techniques to minimize leakage power in idle states?

13. (a) Demonstrate how a carry save adder operates and why it is efficient for multi-operand addition.

Or

(b) Derive the expression for the worst-case delay in a Ripple Carry Adder in terms of the number of bits and the propagation delay of a single full adder.

14. (a) Comprehend the architecture and operation of a multiplier-Accumulator (MAC) unit. Provide examples of applications where MAC units are crucial.

Or

(b) Compare the critical path delays of a Wallace Tree Multiplier and a Dadda Multiplier. Explain how each architecture achieves a reduction in partial products.

15. (a) How do different types of ROM (e.g., Mask ROM, PROM EPROM and EEPROM) vary in their power consumption characteristics and which types are more amenable to low-power designs?

Or

(b) What are some innovative approaches or techniques for low-power precharge and equalization circuit design?

PART C — (1 × 15 = 15 marks)

16. (a) Examine the impact of Technology Scaling on Low Power Circuits.

Or

(b) Differentiate the power consumption of a Ripple Carry Adder and a Carry Look-Ahead Adder. Consider both dynamic and static power components.

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