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Question Paper Code : 20935

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2023.

Fifth Semester

Electronics and Communication Engineering

EC 3552 – VLSI AND CHIP DESIGN

(Common to : Electronics and Telecommunication Engineering)

(Regulations 2021)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. How does MOSFET act as a switch?

2. Realize the 2:1 multiplexer using transmission gates.

3. Draw the stick diagram for 2-input NAND gate.

4. What are the disadvantages of pass transistor logic?

5. Differentiate latches and registers.

6. What are the timing classification of digital system?

7. List the various interconnect parameters analyzed in VLSI chip design.

8. What is the significance of FPGA?

9. Differentiate FPGA design and ASIC design flow.

10. Write the test bench in Verilog HDL to test the D-flip flop.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Obtain the first order model relating the current and voltage (I-V) for an nMOS transistor in three regions of operation. (7)

(ii) Discuss the velocity saturation and mobility degradation of an nMOS transistor under non-ideal I-V effects. (6)

Or

(b) Elucidate the dynamic behaviour of MOSFET and discuss each of the component. (13)

12. (a) (i) Realize the AND gate using pass transistor logic and explain the operation circuit. (6)

(ii) Discuss the disadvantages of dynamic logic gates. Provide the solution to overcome the disadvantages. (7)

Or

(b) (i) Find the Elmore's constant for 4-input NAND gate. (6)

(ii) What are the types of power dissipation in CMOS circuits? Find the total power dissipation and discuss the low power design principles. (7)

13. (a) (i) Explain the multiplexer based latches and master slave edge triggered register. (7)

(ii) Describe the true single phase clock register. (6)

Or

(b) (i) Illustrate the combined effect of skew and jitter in sequential logic circuit and find the time period of the clock. (7)

(ii) Design the sequential logic circuit based on self-timed approach. (6)

14. (a) (i) Write the design techniques in dealing with capacitive cross talk. (6)

(ii) Describe the design techniques available to the designer to address the voltage drop over the inductor problem. (7)

Or

(b) (i) Realize the combinational function with PLA.

$$Y1 = \sum m(2,3,4,6) \qquad Y2 = \sum m(1,2,3,4)$$ (7)

(ii) Elucidate the basic architecture of FPGA. (6)

15. (a) (i) Illustrate the microchip design process and identify the issues in test. (7)

(ii) What are common fault models in CMOS design? With a suitable diagram enlighten the causes of faults. (6)

Or

(b) (i) Explain the automatic test pattern generation with a suitable example. (7)

(ii) Describe the boundary scan with necessary diagrams. (6)

PART C — (1 × 15 = 15 marks)

16. (a) Realize the sum of minterms $F = \sum m(0,1,7,11,15) + \sum d(2,3,5)$ using

(i) Static CMOS logic and (7)

(ii) Clocked CMOS logic. (8)

Or

(b) (i) Apply the concept of 3-stage pipelining to $\log(|a_n + b_n|)$ and find the number clock period for $n=3$ to get the output. (7)

(ii) Design a 4-bit binary to excess-3 code converter using ROM. (8)

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