Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 70499

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2023.

Sixth/Seventh Semester

Electronics and Communication Engineering

EC 8095 — VLSI DESIGN

(Common to : Electrical and Electronics Engineering/Electronics and Instrumentation Engineering/Electronics and Telecommunication Engineering/Instrumentation and Control Engineering/Robotics and Automation)

(Regulations 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Draw the stick diagram of a 3-input NAND gate.

2. Sketch the RC equivalent circuit of a CMOS inverter.

3. Obtain the logical efforts of footed and unfooted domino buffers.

4. What are the sources for gate leakage current in CMOS circuits?

5. State the applications of sense amplifier circuits.

6. Compare the data path for computation of $\log(|a+b|)$ in pipelined and non-pipelined design.

7. Draw the circuit schematic of a mirror adder circuit and mention its significance.

8. Sketch the block diagram of a 4 × 4 multiplier and highlight one possible critical path.

9. How is IDDQ testing performed?

10. List the building blocks of FPGA.

PART B — (5 × 13 = 65 marks)

11. (a) What are the non-ideal effects on I-V characteristics? Obtain the expression for critical electric field including the non-ideal effects.

Or

(b) Obtain the expression for long channel drain current in cutoff, linear and saturation regions.

12. (a) Sketch HI-skew and LO-skew 3-input NAND gate. Determine the logical effort of each gate during its transition.

Or

(b) Elaborate on the sources of static power dissipation in CMOS devices.

13. (a) Discuss the working of pulse registers using

(i) Glitch generation logic (7)

(ii) Flow-through register (6)

Or

(b) Establish the property "*A C^2MOS – based pipeline circuit is race free as long as all the logic functions F between the latches are non-inverting*" using suitable circuit.

14. (a) Design a full adder cell using transmission gates. Use Manchester carry gates to obtain propagate and generate terms of the adder.

Or

(b) Discuss the working of a basic differential sense amplifier circuit. How differential sensing is applied to an SRAM memory column?

15. (a) Explain the parallel scan based testing procedure. List its advantages over serial scan chains.

Or

(b) Elaborate on the role played by pseudo-random sequence generator during execution of BIST.

PART C — (1 × 15 = 15 marks)

16. (a) Sketch a 3-input symmetric NOR gate. Size the inverters so that the pull-down is four times as strong as the net worst-case pull-up. Label the transistor widths. Estimate the rising, falling, and average logical efforts. How do they compare to a static CMOS 3-input NOR gate?

Or

(b) When adding two unsigned numbers, a carry-out of the final stage indicates an overflow. When adding two signed numbers in two's complement format, overflow detection is slightly more complex. Develop a Boolean equation for overflow as a function of the most significant bits of the two inputs and the output.