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Question Paper Code : 50440

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2017
Fourth Semester
Electronics and Communication Engineering
EC 6404 – LINEAR INTEGRATED CIRCUITS
(Common to Medical Electronics/Robotics and Automation Engineering)
(Regulations 2013)

Time : Three Hours

Maximum : 100 Marks

Answer ALL questions

PART – A (10×2=20 Marks)

1. Draw the dc transfer characteristics of a BJT differential amplifier and define differential mode input voltages.
2. The power supply rejection of an op-amp is 80dB for a 1V change in supply voltage. Calculate the change in offset voltage.
3. State the limitations of an ideal integrator.
4. How will you realize a peak detector using a precision rectifier ?
5. Mention the need of pre-distortion circuits in Gilbert analog multiplier and how is the configuration of Gilbert multiplier done with pre-distortion circuits.
6. Define capture-range and lock-range of PLL.
7. How is the classification of A/D converters carried out based on their operational features ?
8. Find the number of resistors required for an 8-bit weighted resistor D/A converter. Consider the smallest resistance is R and obtain those resistance values.
9. Define current transfer ratio of an opto-coupler.
10. Draw a fixed voltage regulator circuit and state its operations.



PART – B

(5×13=65 Marks)

11. a) i) With a help of a block diagram, explain the various stages present in an operational amplifier. (6)
- ii) Draw the transfer characteristics of an operational amplifier and explain the linear and non-linear operation. (7)
- (OR)
- b) i) Draw the inverting and non-inverting amplifier circuits of an op-amp in closed-loop configuration. Obtain the expressions for the closed-loop gain in these circuits. (8)
- ii) Perform the AC analysis of the operational amplifier 741. (5)
12. a) i) For performing differentiation in an operational amplifier, integrator is preferred to differentiator – Explain. (6)
- ii) What is an instrumentation amplifier? Draw a system whose gain is controlled by a variable resistance. (7)
- (OR)
- b) i) Design a clipper circuit for a clipping level of +0.61V, given an input sine wave signal of 0.5V peak. Assume the gain of the amplifier is 12 and it has an input resistance of 1k-ohm connected. (7)
- ii) Design a second order Butterworth low-pass filter having upper cut-off frequency of 2.5 kHz. (6)
13. a) i) Write notes on basic analog multiplication techniques. (5)
- ii) Explain the operation of a variable transconductance multiplier circuit. Derive the expression for its output voltage. (8)
- (OR)
- b) i) Derive the expression for free running frequency of voltage controlled oscillator. (5)
- ii) Explain the process of FSK demodulation using PLL. How is the stability of the frequency obtained in a PLL by the use of voltage controlled oscillator? (8)
14. a) i) Explain in detail on the operational features of 4-bit weighted resistor type D/A converter. (7)
- ii) Differentiate between current mode and voltage mode R-2R ladder D/A converters. (6)

(OR)



- b) i) With a neat block diagram, explain the operation of successive approximation type A/D converter in detail. (5)
- ii) An 8-bit A/D converter accepts an input voltage signal of range 0 to 9V. What is the minimum value of the input voltage required for generating a change of 1 least significant bit? Specify the digital output for an input voltage of 4 V. What input voltage will generate all 1s at the A/D converter output? (8)
15. a) i) With neat diagram, explain the operation of an astable and monostable multivibrators. (8)
- ii) Draw the functional diagram and connection diagram of a low voltage regulator and explain. (5)
- (OR)
- b) i) Draw the block diagram of a typical IC audio power amplifier and briefly explain their salient features. (6)
- ii) Design a frequency to voltage converter using IC VFC 32 for a full scale output of 8 V for a full scale input frequency of 80 kHz with a maximum ripple of 8 mV. (7)

PART – C

(1×15=15 Marks)

16. a) i) Design a differentiator to produce an output of 4 V when the input changes by 2 V in 60 micro seconds. (5)
- ii) A PLL has a free running frequency of 400 kHz and the band-width of the low pass filter is 8 kHz. Will the loop tend to acquire lock for an input signal of 550 kHz? Explain. In this case, assume that the phase detector produces sum and difference frequency components. (10)
- (OR)
- b) i) Design a square wave generator using 555 timer for a frequency of 120 Hz and 60% duty cycle. Assume $C = 0.2 \mu\text{F}$. (7)
- ii) For a 4-bit R-2R ladder D/A converter assume that the full scale voltage is 12 V. Calculate the step change in output voltage on input varying from 1001 to 1111. (8)