



PART - B (5 × 16 = 80 marks)

11. (a) Simplify the following Boolean function F, using Quine McCluskey method and verify the result using K-map  $F(A, B, C, D) = \Sigma (0, 2, 3, 5, 7, 9, 11, 13, 14)$  (16)

OR

- (b) (i) Draw and explain Tri-state TTL inverter circuit diagram with its operation. (10)

- (ii) Implement the following function using NAND and inverter gates. (6)

$$F = AB + A'B' + B'C$$

12. (a) (i) Design a 4-bit magnitude comparator with 3 outputs :  $A > B$ ,  $A = B$ ,  $A < B$ . (8)

- (ii) Design a 4 bit binary to gray code converter. (8)

OR

- (b) (i) Implement the following Boolean function using  $8 \times 1$  Multiplexers. (8)

$$F(A, B, C, D) = \Sigma (1, 3, 4, 11, 12, 13, 14, 15)$$

- (ii) Explain the concept of carry look ahead adder with neat logic diagram. (8)

13. (a) Design a 3-bit synchronous counter using D-flip flop. (16)

OR

- (b) (i) Draw and explain the 4-bit SISO, SIPO, PISO and PIPO shift register with its waveforms. (12)

- (ii) Realize D flip-flop using SR flip-flop. (4)

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14. (a) (i) Implement the following function using PLA. (12)

$$F1(x, y, z) = \Sigma m(1, 2, 4, 6)$$

$$F2(x, y, z) = \Sigma m(0, 1, 6, 7)$$

$$F3(x, y, z) = \Sigma m(2, 6)$$

- (ii) Write short notes on FPGA. (4)

OR

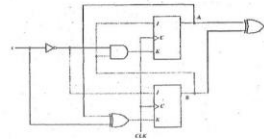
- (b) (i) Explain memory READ and WRITE operation with neat timing diagram. (8)

- (ii) Explain the organization of ROM with relevant diagrams. (8)

15. (a) Design an asynchronous sequential circuit with two inputs  $X_1$  and  $X_2$  and with one output Z. When  $X_1$  is 0, the output Z is 0. The first change in  $X_2$  that occurs while  $X_1$  is 1 will cause output Z to be 1. The output Z will remain 1 until  $X_1$  returns to 0. (16)

OR

- (b) Construct the transition table, state table and state diagram for the more sequential circuit given below. (16)



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