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Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 50473

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2017

Third Semester

Electrical and Electronics Engineering

EE 6301 – DIGITAL LOGIC CIRCUITS

(Common to Electronics and Instrumentation Engineering/Instrumentation and Control Engineering)

(Regulations 2013)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. Convert $(115)_{10}$ and $(235)_{10}$ to hexadecimal numbers.
2. What is a gray code and mention its advantages.
3. What is a K-map ?
4. Compare decoder and demultiplexer.
5. What do you mean by race around condition in a flip-flop ?
6. What is a preset table counter and ripple counter ?
7. What happens to the information stored in a memory location after it has been read and write operation ?
8. What is Programmable Logic Array ?
9. Define modularity.
10. What are the languages that are combined together to get VHDL language ?

PART – B (5×13=65 Marks)

11. a) Explain in detail about error detecting and error correcting code. (13)

(OR)

b) Write short notes on following : (13)
i) RTL ii) DTL iii) TTL and iv) ECL

12. a) I) Plot the logical expression $ABCD + A\bar{B}\bar{C}\bar{D} + A\bar{B}C + AB$ on a 4-variable K-map; obtain the simplified expression from the map. (7)

II) Express the function $Y = A + \bar{B}C$ in canonical SOP and canonical POS form. (6)

(OR)

b) Design a 4-bit gray code to binary converter and express using logic gates. (13)

13. a) Explain the operation, state diagram and characteristics of T-flip-flop and master-slave JK flip-flop. (13)

(OR)

b) Explain in detail about different shift registers. (13)

14. a) Discuss about the hazards in asynchronous sequential circuit and the ways to eliminate them. (13)

(OR)

b) I) Write short notes on PLA and PAL. (7)

II) What is hazards ? Explain hazards in digital circuits. (6)

15. a) Write a VHDL code to realize a full adder using behavioural modeling and structural modeling. (13)

(OR)

b) I) Discuss briefly the packages in VHDL. (6)

II) Write an VHDL coding for realization of clocked SR flip-flop. (7)

PART – C (1×15=15 Marks)

16. a) Design an asynchronous sequential circuit with two inputs x_1 and x_2 and one output Z. Initially, both inputs are equal to zero. When x_1 or x_2 becomes 1, the output Z becomes 1. When the second input also becomes 1, the output changes to 0. The output stays at 0 until the circuit goes back to the initial state. (15)

(OR)

b) I) Design a full adder using 4×1 multiplexer, also write its truth table and draw the logical diagram. (8)

II) Describe level triggering and edge triggering. (7)